Design and Implementation of Ternary Logic Gates over a Quaternary Logic

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Abstract – Ternary logic is MVL compliant. However, only three logic states are used "0", "1" and "2". The optimum radix (r) of a fractional number is found to be the natural logarithm (e). Ternary logic uses number representation with r=3, compared to quaternary logic which uses r=4, hence the most economical integer radix which is the closest to the natural logarithm e, is base 3 [3]. This special property of base 3 inspired the early computer designers to build a ternary computer. According to the ITRS1 we will face the brick wall in 2015 if we continue in the same development speed. So we have to come up with other solutions, and MVL is one of most promising one. MVL can in principle increase data processing capability per unit chip area in the future. It is true that the noise margins are a serious issue, which is the reason why my solutions are ternary. This will keep the noise margins at an acceptable level. In 2004, a research team in Rennes made a MVL Chip using Supplementary Symmetrical. The application of MVL to asynchronous circuits can be an effective way to the design of low power high-performance VLSI digital circuits [6].

Index Terms – MVL, BT, RSFG, STI, NTI, PTI.

1. INTRODUCTION

Multiple-valued logic (MVL) has in the last few decades been proposed as a possible substitute of binary logic. While binary logic is limited to only two states, "true" or "false", multiple-valued logic (MVL) can replace these with finitely or infinitely numbers of values. A MVL system is defined as a system operating on a higher radix than two [1]. A radix-n set has n elements, 0, 1...n − 1. The practicability of MVL depends on the accessibility of the devices constructed for MVL operations [2]. The devices should be able to switch between the different logical levels, and preferably be less complex than the binary counterparts.

Three-valued, or ternary, logic offers several important advantages over binary logic in the design of digital systems [4]. For example, more information can be transmitted over a given set of lines or stored for a given register length, the complexity of interconnections can be reduced, reduction in chip area can be achieved, and more efficient error-detection and error-correction codes can be employed. Furthermore, serial and some serial-parallel arithmetic operations can be carried out at higher speeds. Most of these advantages have a direct bearing on the VLSI implementation of digital systems, and as a result several realizations of basic ternary gates have been proposed in the literature [2]–[7]. These have been shown to be useful for the design of "ternary computers," for digital filtering [5,8], and for various other applications [1]-[9]. The application of MVL to asynchronous circuits can be an effective way to the design of low power high-performance VLSI digital circuits [6].

2. RELATED WORK

1.1 K. C. Smith covers the role of multivalued logic (MVL) in the binary world. This tutorial places the developments and potential of multiple-valued signals and logic in the relevant context of binary and two-valued signals; multivalued representation; binary-related radices; multivalued functions; storage techniques in MVL; and implementation issues. An overview of applications is included [1].

The characteristics of the successful m-valued I ^{2}L and ROMs that have been designed in the past are examined, and the reasons for their success are discussed in this paper by D. Etiemble. The problems associated with scaling of m-valued CMOS current mode circuits are examined. The tolerance issue, the respective propagation delays of binary and m-valued ICs, and the interconnection issue are considered. The challenges for m-valued circuits in competition with the exponential performance increase of binary circuits are identified [2].

1.2 B. Hayes presents a multiplier circuit using balanced ternary (BT) notation. The multiplier can multiply both negative and positive numbers, which is one of the advantage able properties of the balanced ternary numbering systems. By using balanced ternary notation, it is possible to take advantage of carry free multiplication, which is exploited in designing a fast multiplier circuit. The circuit is implemented with

recharged semi-floating gate (RSFG) devices. The circuit operates at 1 GHz clock frequency at a supply voltage of only 1.0 Volt. The circuit is simulated by using Cadencereg Analog Design Environment, with CMOS090 process parameters, a 90nm general purpose bulk CMOS process from STMicroelectronics with 7 metal layers [3].

1.3 K. C. Smith View Advances in multiple-valued logic (MVL) has been inspired, in large part, by advances in integrated circuit technology. Multiple-valued logic has matured to the point where four-valued logic is now part of commercially available VLSI IC's. Besides reduction in chip area, MVL offers other benefits such as the potential for circuit test. This paper describes the historical and technical background of MVL, and areas of present and future application. It is intended, as well, to serve as a tutorial for the non specialist [4].

1.4 X.W. wu, Prof. F.P. Prosser, reviews the main difficulties and advantages in developing CMOS ternary circuits. In addition to employing multiple power sources and multiple thresholds, we describe a new theory of transmission functions for designing CMOS ternary logic circuits. It can explain the main CMOS ternary circuits proposed previously. Computer simulations show that the circuits based on the transmission-function theory have more desirable transfer characteristics than ones with resistors [5].

1.5 R. Mariani1, F. Pessolano2, R. Saletti1 shows a new approach to low-power low-voltage CMOS Multiple- Valued (MVL) Ternary Logic, the "complete model". This logic uses standard tec an original characterization of CMOS multivalued dynamic gates, it is shown as the advantages obtained are better noise margins and a lower power consumption as compared to other CMOS ternary solutions. As application of this approach, it is then discussed how general purpose asynchronous circuits can be designed with complete model ternary logic elements [6].

1.6 H. T. Mouftah and K. C. Smith has proposed a method of design of three-valued logic circuits which reduces the need for complementary pairs of M.O.S. integrated circuits is presented. Circuits of basic ternary operators (inverters, NAND and NOR) are utilizing single M.O.S. transistors. Based on these ternary operators it is possible to design simpler and cheaper three-valued logic systems. As examples, the construction of the Jk arithmetic circuit and the T-gate are described [7].

3. PORPOSED MODELLING

3.1BASICS OF TERNARY LOGIC

The history of Multi-Valued Logic as a separate topic began in the early 1920s by Polish philosopher Jan Lukasiewicz (1878-1956). His objective was to introduce a third additional truth-value for "possible". The outcome of this research is known as the Lukasiewicz systems or the ternary predicate calculus. Parallel to the approach of Lukasiewicz, the American mathematician Dr. Emil Leon Post (1897-1954), born in Bialystok in Poland, introduced the idea of several additional truth degrees, and used this approach to solve the problem of the represent ability of functions, also known as the Post Algebra.

3.2PROPOSED TERNARY INVERTE

We proposed three basic ternary elements the STI (Simple Ternary Inverter), the NTI (Negative Ternary Inverter) and the PTI (Positive Ternary Inverter), whose logic functions are shown in Table [9].

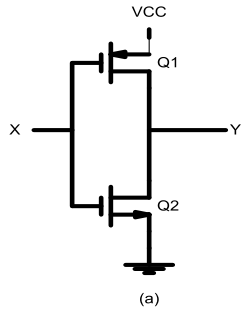


Figure 3.1: Proposed Ternary Inverter

3.3STI: Standard Ternary Inverter

Figure 2.1 shows the design of a standard ternary inverter (STI).When the input X is 0 the NMOS transistor is OFF and the PMOS transistor is ON thus the output Y is pulled up to 1 because it is connected to VDD. Conversely, when X is 1, the NMOS is ON, the PMOS is OFF and the Y is pulled down to O. When X is 1/2 both the transistor may off and output Y is 1/2 nothing but the input A. The only current flow in either case is the very small leakage current of the reverse bias source and drain junctions. The most significant feature of these circuits is that the current drawn from the power supply in both of these operating points is nearly equal to zero.

3.4. PTI: A Positive Ternary Inverter

Figure shows the design of a positive ternary inverter (PTI). The gate of PMOS is connected to negative power supply to keep it constantly turn on and the output Y is pulled up to1 when the input is 1/2. The output of a standard CMOS inverter by altering the length-to-width ratio of the PMOS and NMOS channels can significantly change the resistance of channels. Thus, the resistance of the circuit is directly proportional to its L/W ratio which can be effectively used to change the resistance of transistors to suit design needs.

By equalizing the transfer parameter βp and βn of the PMOS and NMOS transistor i.e. $\frac{\beta p}{\beta n}$ >1/2, the inverter is HI-skewded which has stronger PMOS transistor. Therefore, the input A ½

we would expect the output will be greater than VDD/2.The gates are usually skewed up by adjusting the width of transistor while maintain minimum length for speed.

3.5. NTI: A Negative Ternary Inverter

Figure shows the design of a negative ternary inverter (NTI). The gate of NMOS is connected to positive power supply to keep it constantly turn on and the output Y is pulled up to 0 when the input is 1/2.

By equalizing the transfer parameter βp and βn of the PMOS and NMOS transistor i.e. $\frac{\beta p}{\beta n}$ <1/2, the inverter is LI-skewded which has stronger NMOS transistor .Therefore, the input X is 1/2 we would expect the output will be lesser than VDD/2.

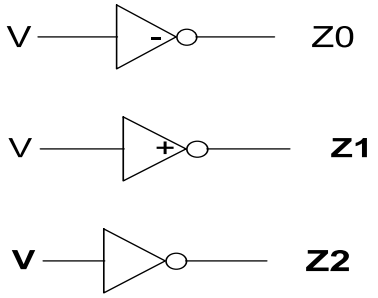


Figure 3.3: Symbolic Representation of (a) NTI (b) PTI (c) STI

Table 2.1: Truth Table of STI

INPUT	OUTPUT
0	1
½	½
1	0

Table 2.2: Truth Table of PTI

INPUT	OUTPUT
0	1
½	1
1	0

Table 2.3: Truth Table of NTI

INPUT	OUTPUT
0	1
½	0
1	0

3.6. T gate ternary function control signal generator circuit

One of the most important functions in MVL is the T gate ternary function control signal generator circuit [11]. This divides logic level in multi-valued logic into a binary state at an arbitrary threshold. This circuit consist of combination of the PTI and NTI for ternary logic and inverted output of the PTI and output of the NTI is given to the AND gate. We used the output of the NTI, inverted output of the PTI and AND gate output (of the PTI and NTI) as a control signal. where Vin can take values of logic 0, logic 1/2 and logic 1 which corresponds to higher level (1), middle level (0) and lower level (- 1), respectively. The block diagram of a T gate ternary function control signal generator circuit is shown in figure 4.6

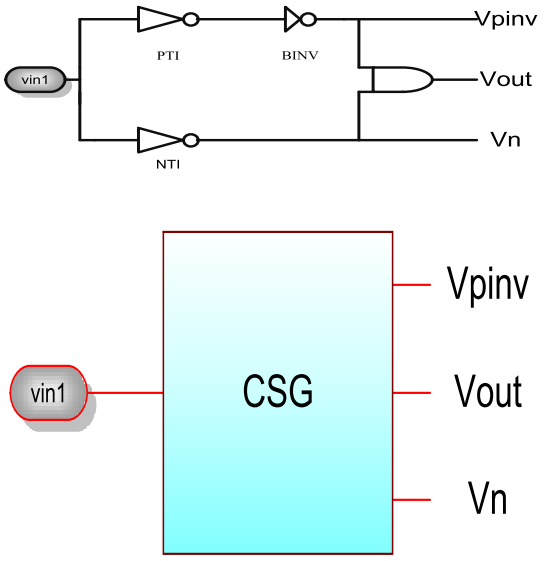
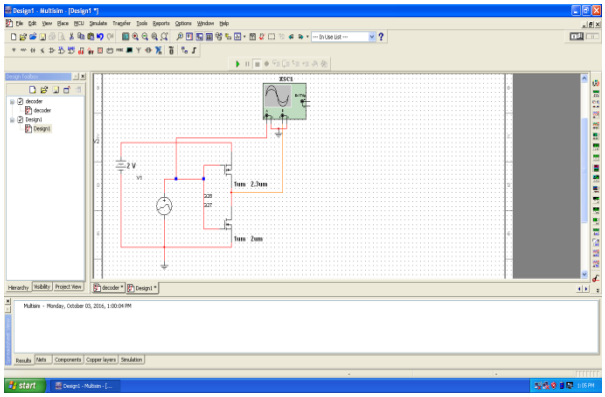


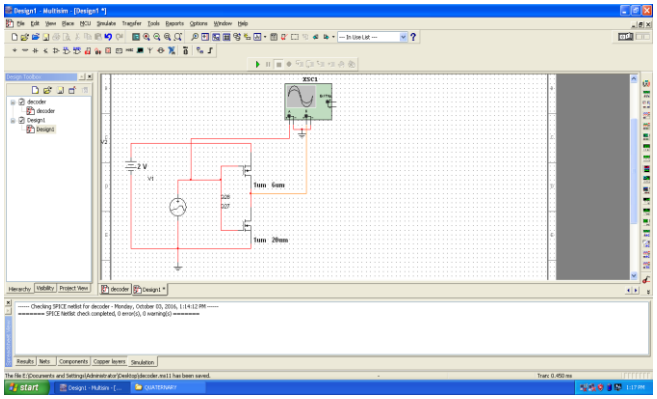
Figure 3.4: T Gate Ternary Function Control Signal Generator Circuit

4. RESULTS AND DISCUSSIONS

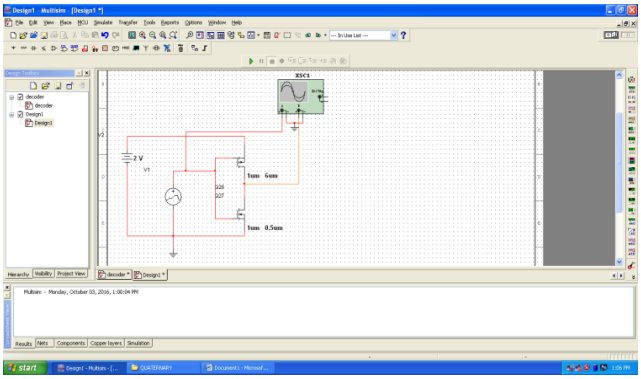
4.1 Implementation of Standard Ternary Inverter



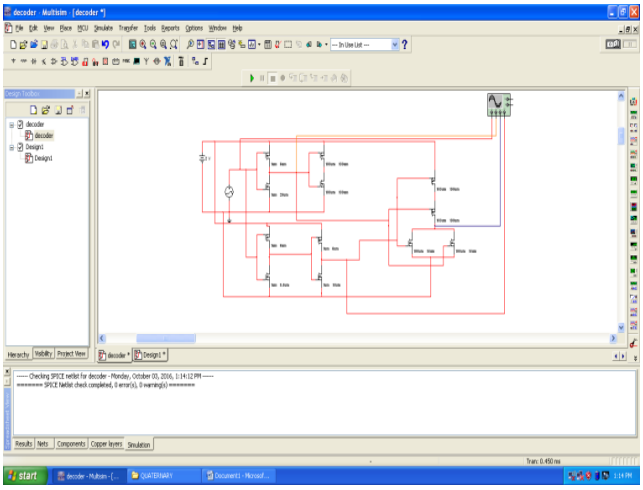
4.2 Implementation of Positive Ternary Inverter



4.3 Implementation of Negative Ternary Inverter



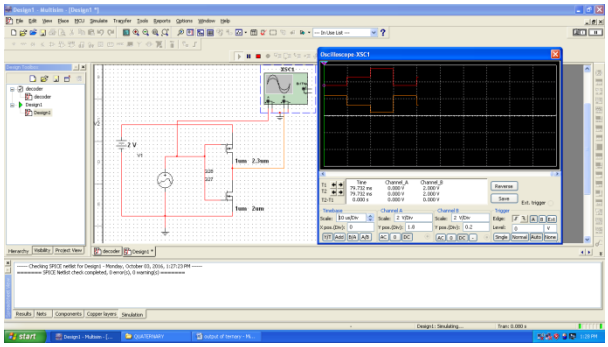
4.4. Implementation of T-Gate Ternary Function CSG



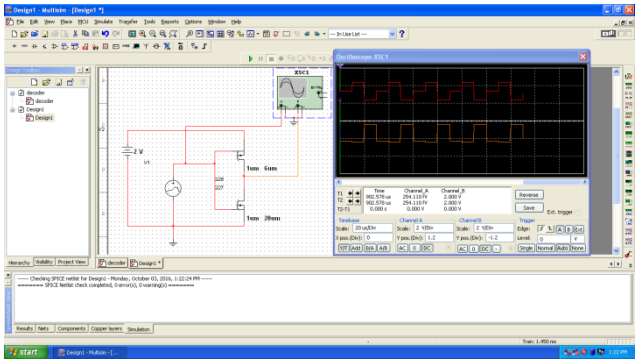
4.5 SIMULATION RESULTS

As technology and competition accelerate, so do the challenges of getting to market first, with better, smaller, and faster products. Today, it is critical for engineers to be productive and effective. Efficiently exploring different design possibilities requires powerful tools and methodologies.

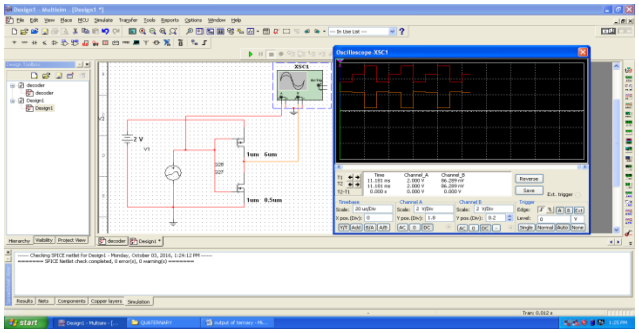
4.5.1. Simulation Result of STI



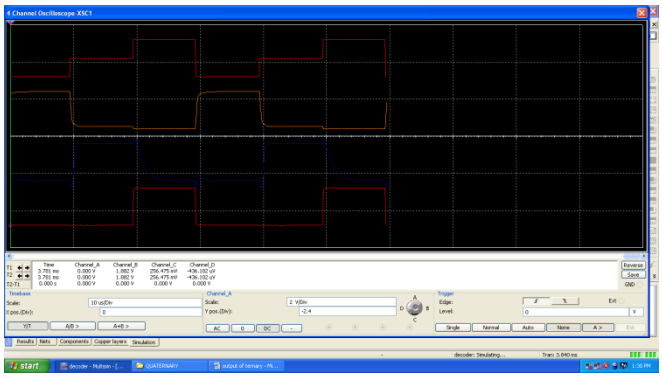
4.5.2. Simulation Result of PTI



4.5.3. Simulation Result of NTI



4.5.4 Simulation Result of T –gate CSG



5. CONCLUSION

We have design basic ternary logic gates and using this gate we also design combinational circuits .first we proposed ternary inverter which is comprised set of a standard ternary inverter, positive ternary inverter and negative ternary inverter with a power supply of 1V. The PTI and NTI have been designed using an inverter and altering the width and length of PMOS & NMOS Of inverter. The design of PTI and NTI is fully compatible with current CMOS technology. All proposed design has very low power dissipation and have very sharp output characteristic compared to their binary counterparts.

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